CS221: Logic Design

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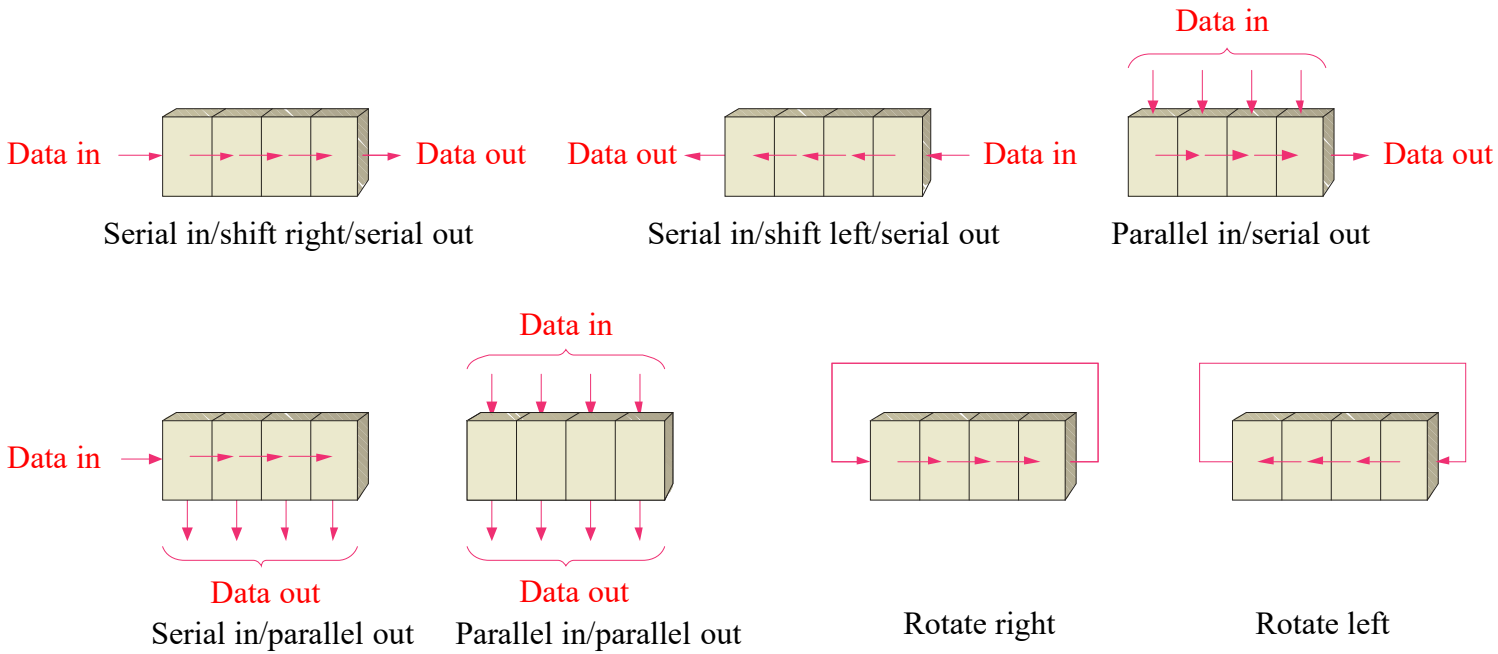
Digital Fundamentals

CHAPTER
Shift Registers

Shift Registers

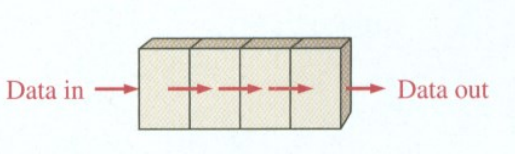
Basic Shift Register Operations

A shift register is an arrangement of flip-flops with important applications in storage and movement of data. Some basic data movements are illustrated here.



Shift Registers

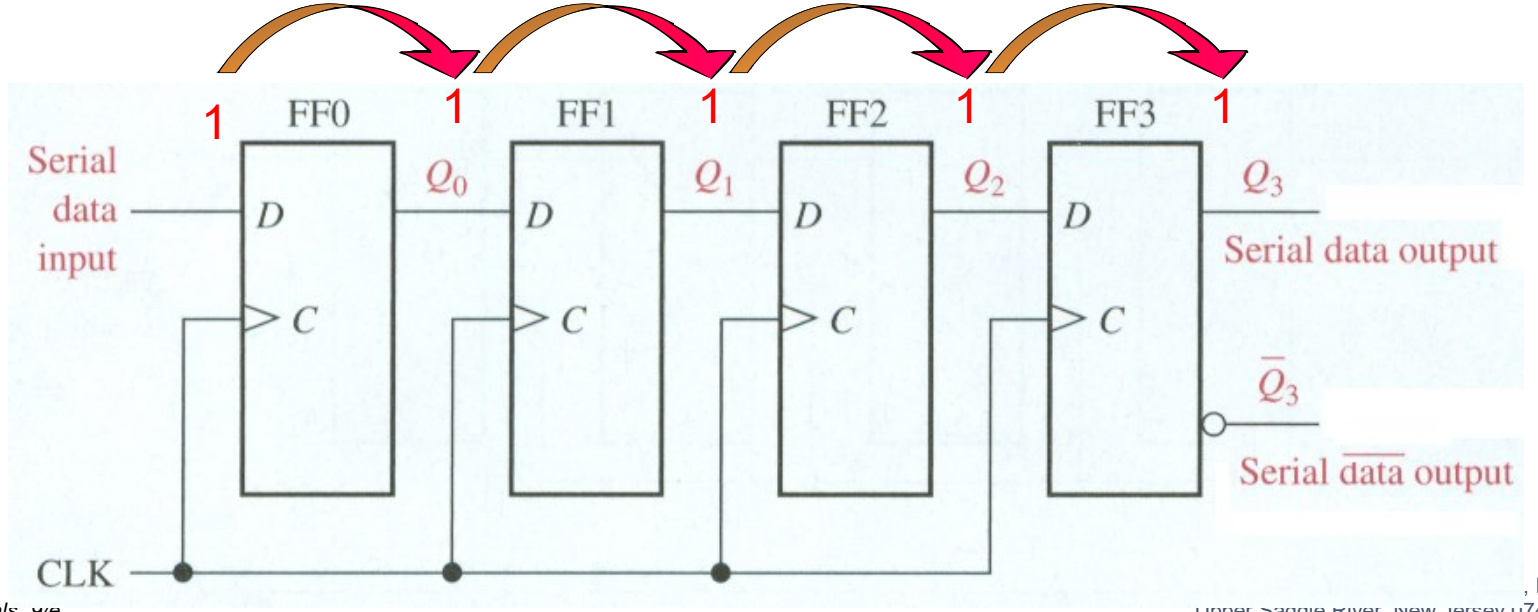
Serial-in/Serial out Shift Register



Shift registers are available in IC form or can be constructed from discrete flip-flops as is shown here with a five-bit serial-in serial-out register.

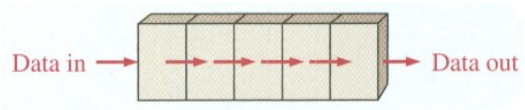
Each clock pulse will move an input bit to the next flip-flop.

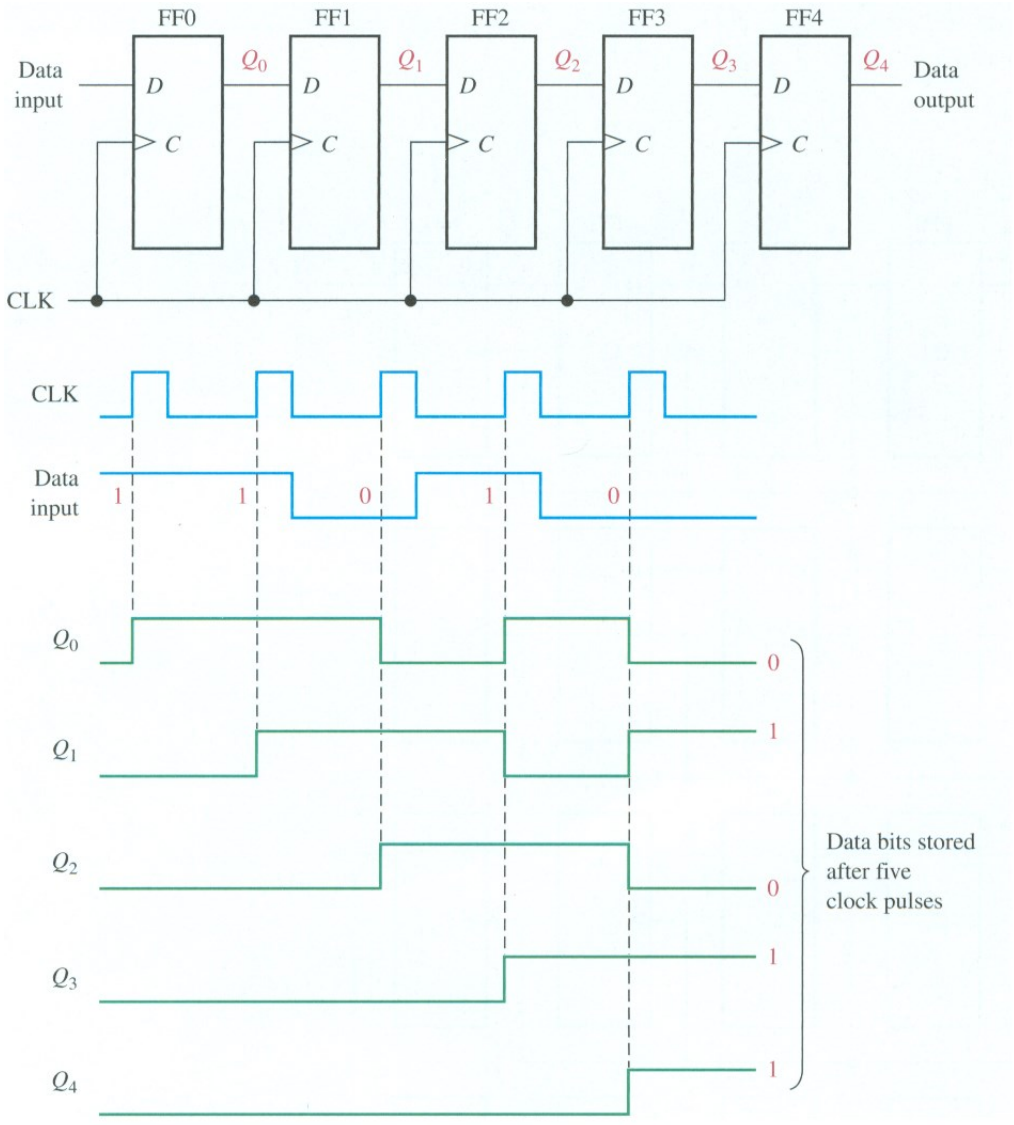
For example, a 1 is shown as it moves across.



Shift Registers

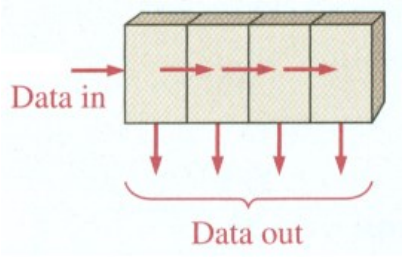
Serial-in/Serial out Shift Register



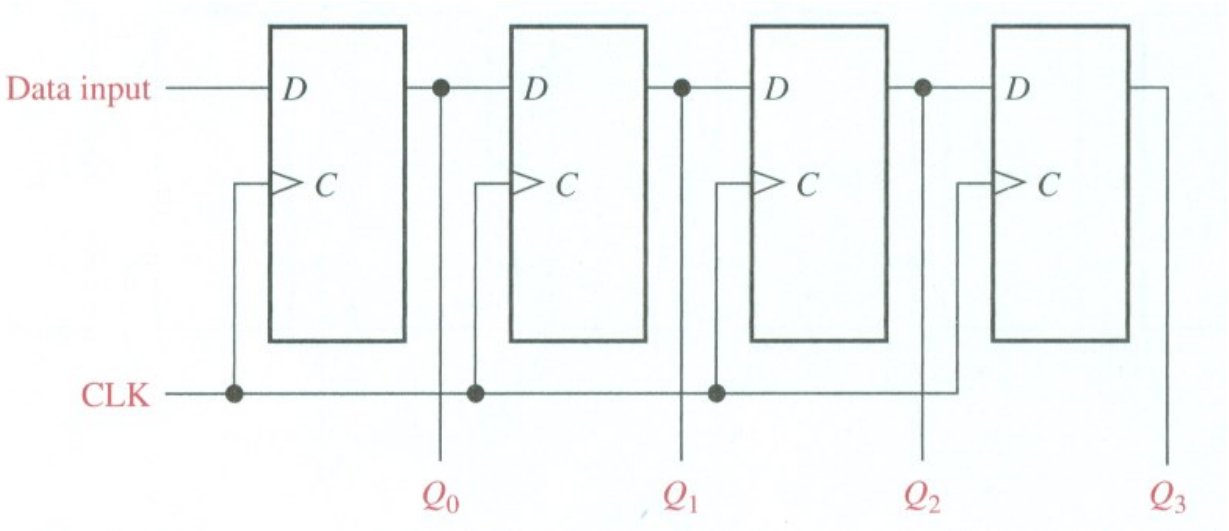


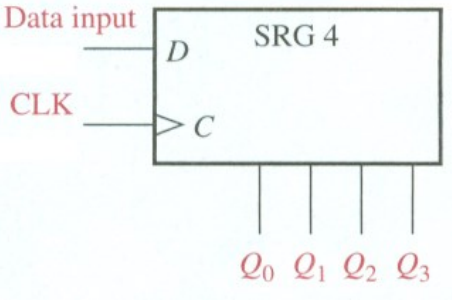
Shift Registers

Serial in/Parallel out Shift Register



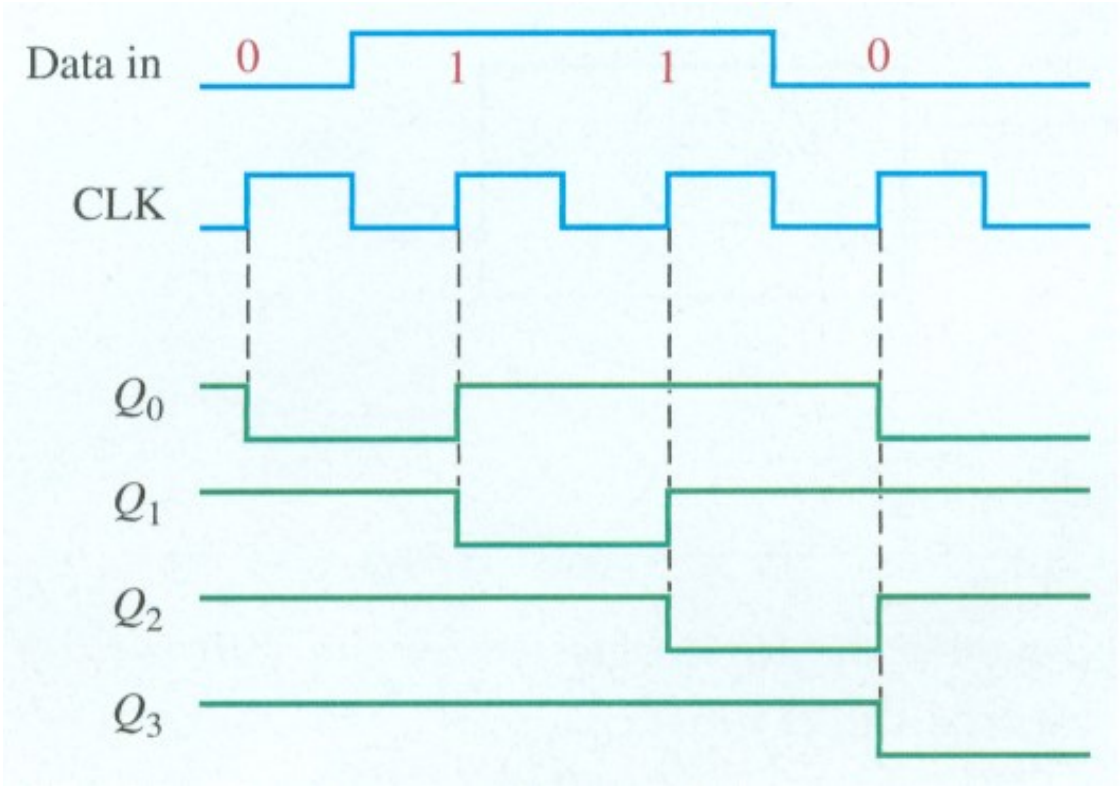
An application of shift registers is conversion of serial data to parallel form.

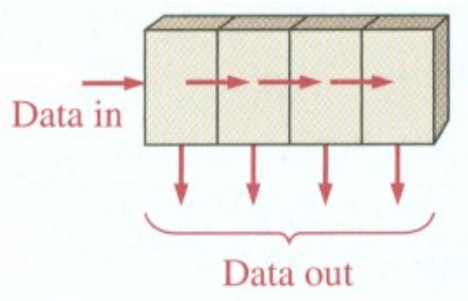


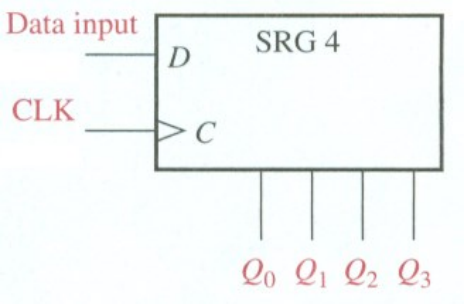


Shift Registers

Serial in/Parallel out Shift Register

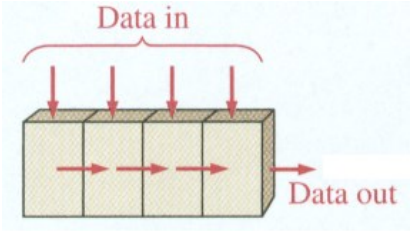




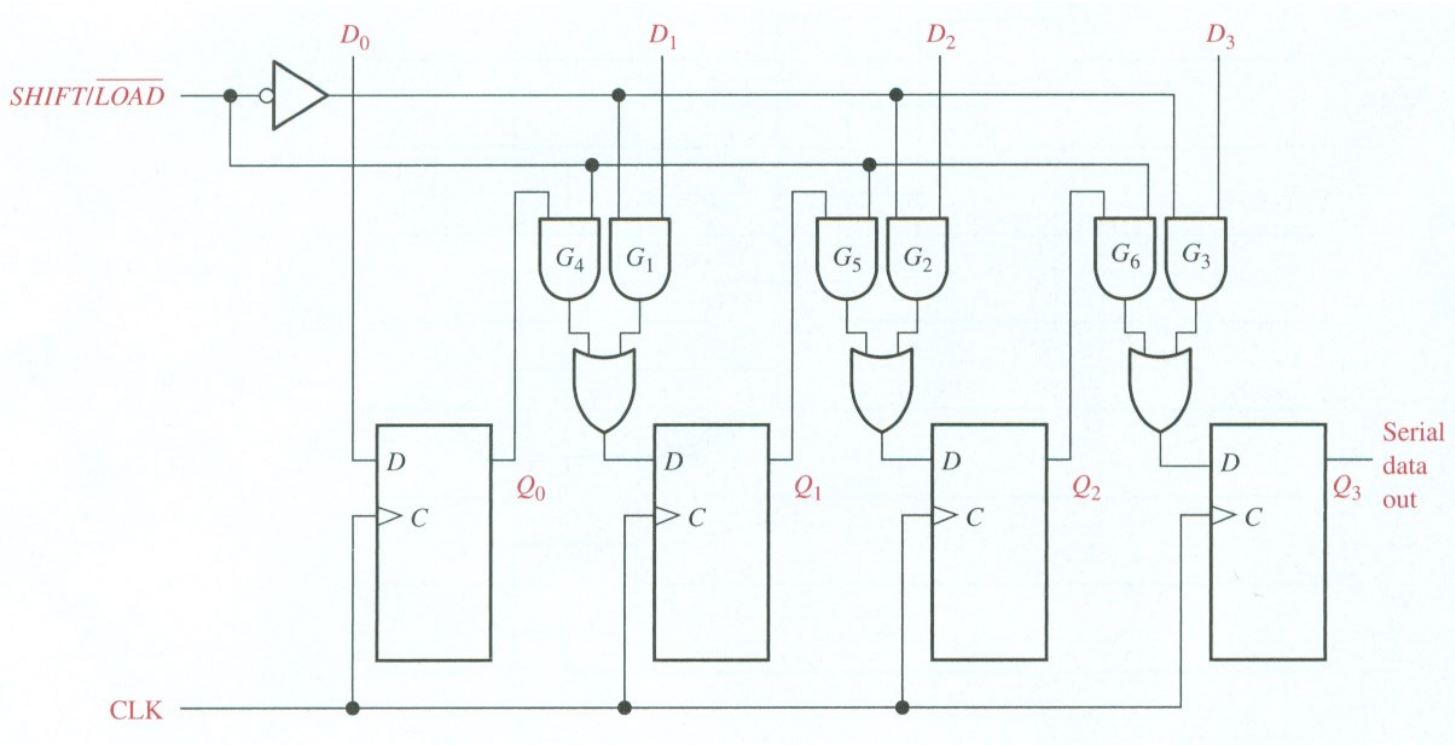


Shift Registers

Parallel in/Serial out Shift Register

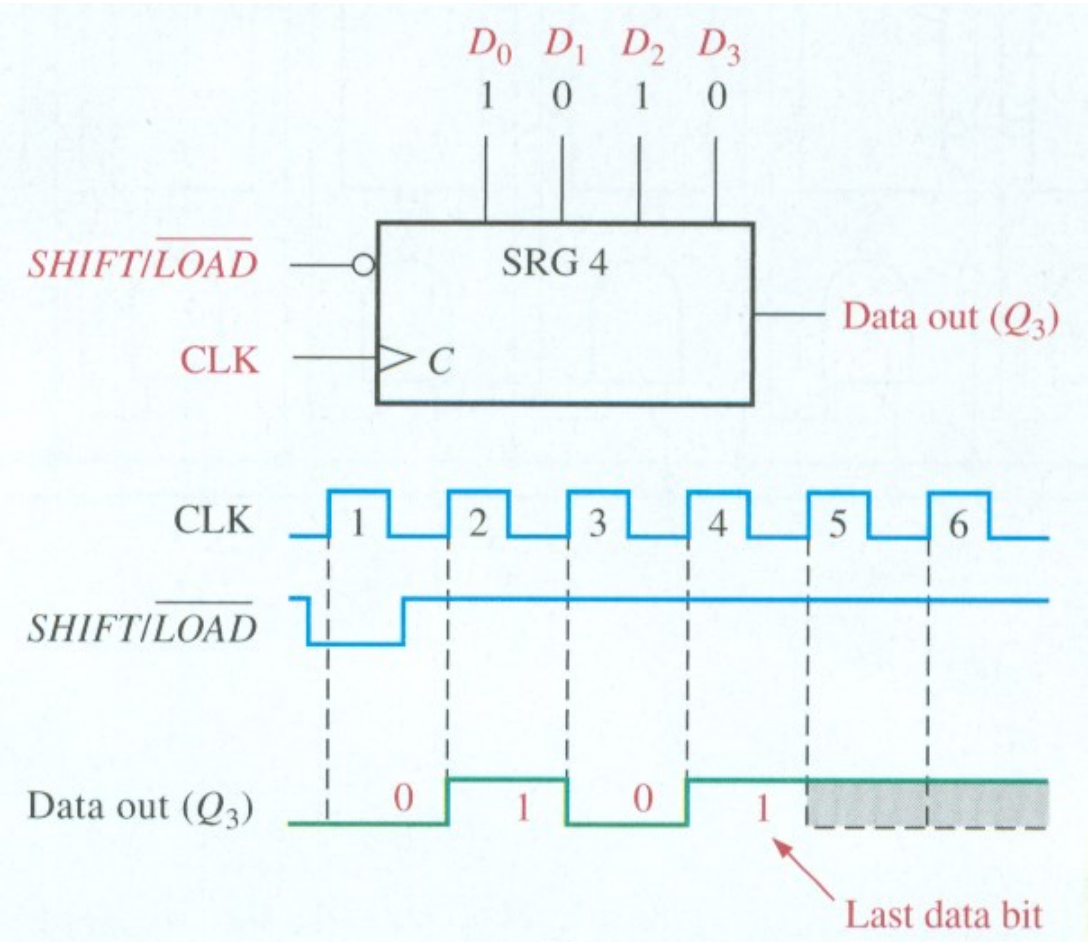


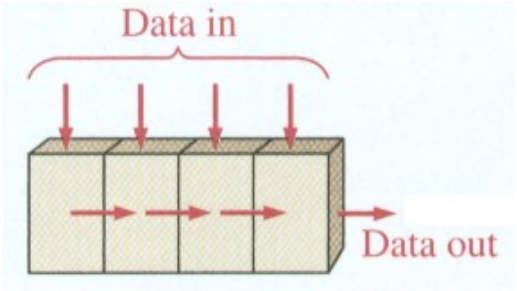
An application of shift registers is conversion of parallel data to serial form.



Shift Registers

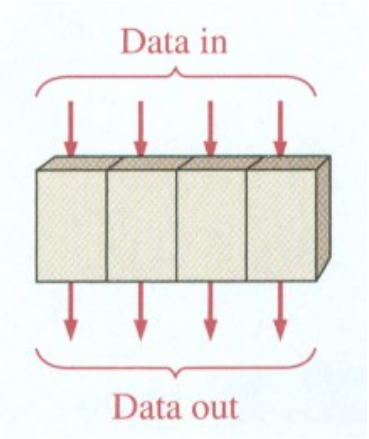
Parallel in/Serial out Shift Register

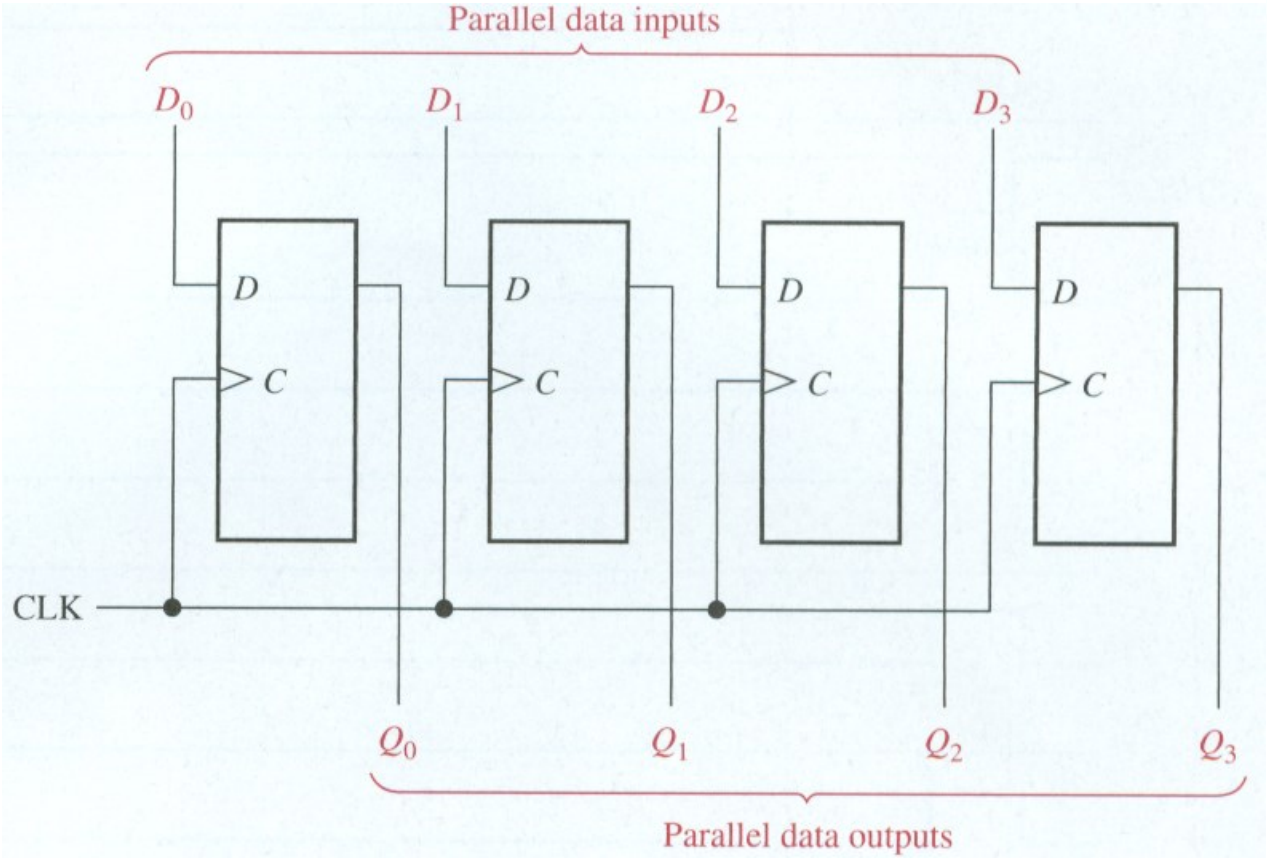




Shift Registers

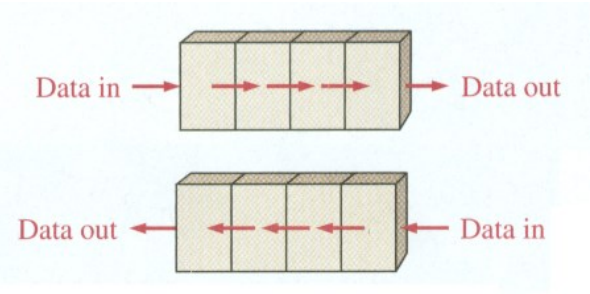
Parallel in/Parallel out Shift Register



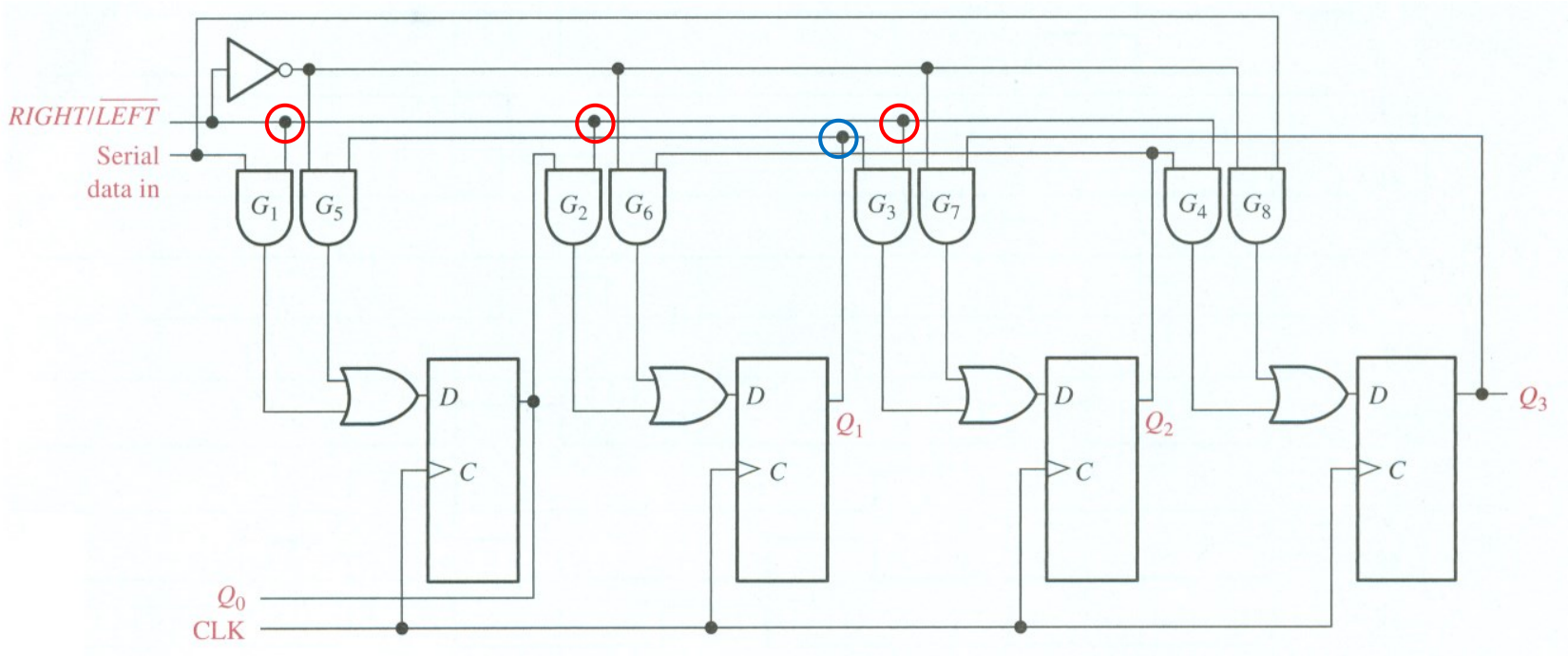


Shift Registers

Bidirectional Shift Register



Bidirectional shift registers can shift the data in either direction using a *RIGHT/$\overline{LEFT}$* input.

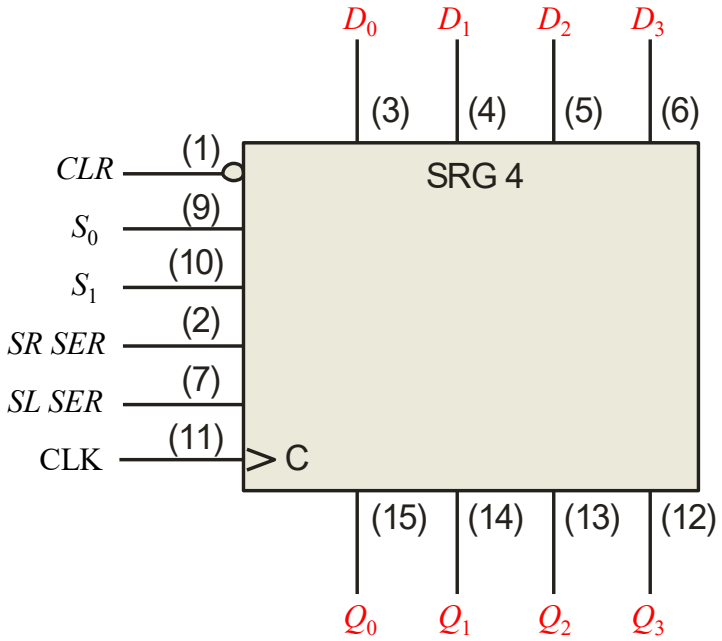


Shift Registers

Universal Shift Register

A universal shift register has both serial and parallel input and output capability.

The 74HC194 is an example of a 4-bit bidirectional universal shift register.



Shift Registers

Shift Register Applications

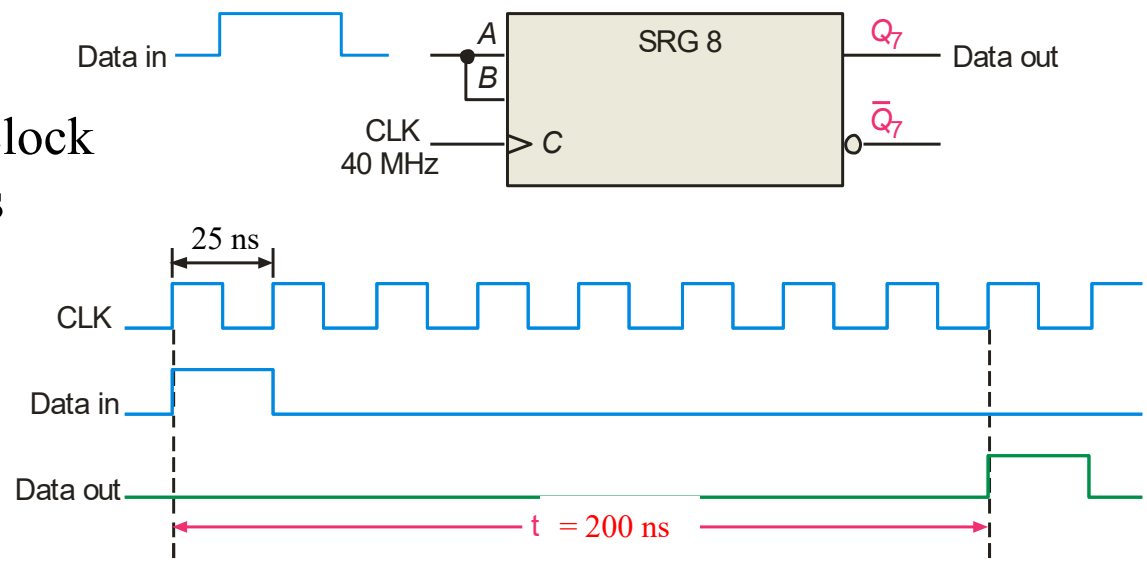
Shift registers can be used to delay a digital signal by a predetermined amount.

Example An 8-bit serial in/serial out shift register has a 40 MHz clock. What is the total delay through the register?

Solution

The delay for each clock is 1/40 MHz = 25 ns

The total delay is 8 x 25 ns = 200 ns

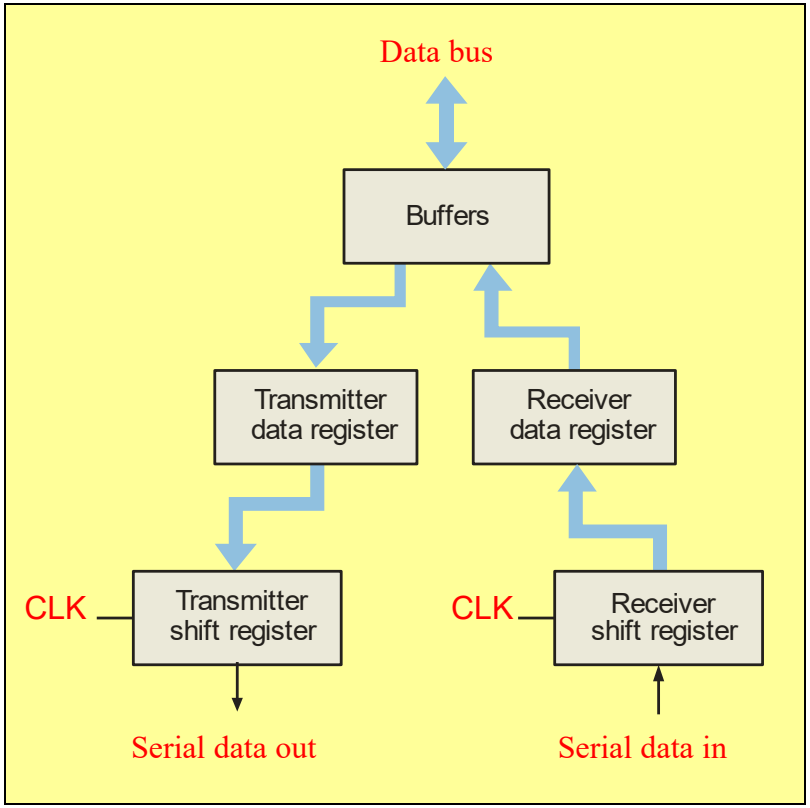


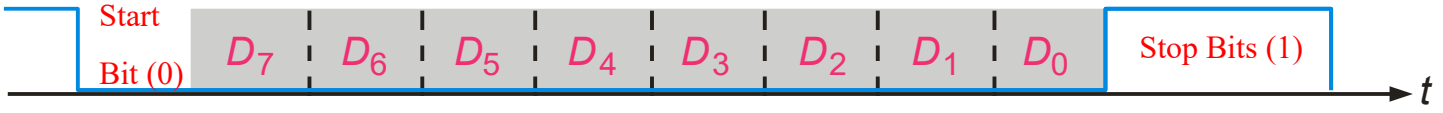
Shift Registers

Shift Register Applications

A UART (Universal Asynchronous Receiver Transmitter) is a serial-to-parallel converter and a parallel to serial converter.

UARTs are commonly used in small systems where one device must communicate with another. Parallel data is converted to asynchronous serial form and transmitted. The serial data format is:





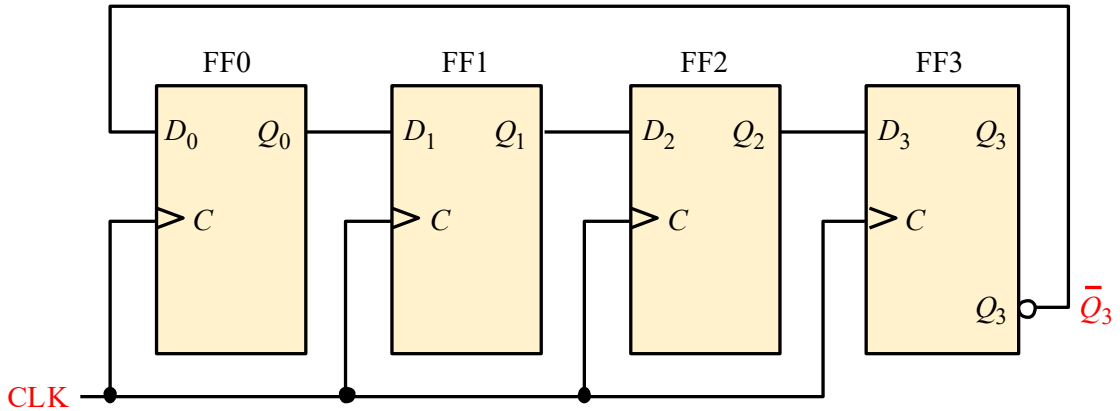
Shift Registers

Inputs		Outputs		
D	CLK	Q	$\overline{Q}$	Comments
1	↑	1	0	SET
0	↑	0	1	RESET

Shift Register Counters

Shift registers can form useful counters by recirculating a pattern of 0's and 1's. Two important shift register counters are the *Johnson counter* and the *ring counter*.

The Johnson counter is useful when you need a sequence that changes by only one bit at a time but it has a limited number of states ($2n$, where n = number of stages).



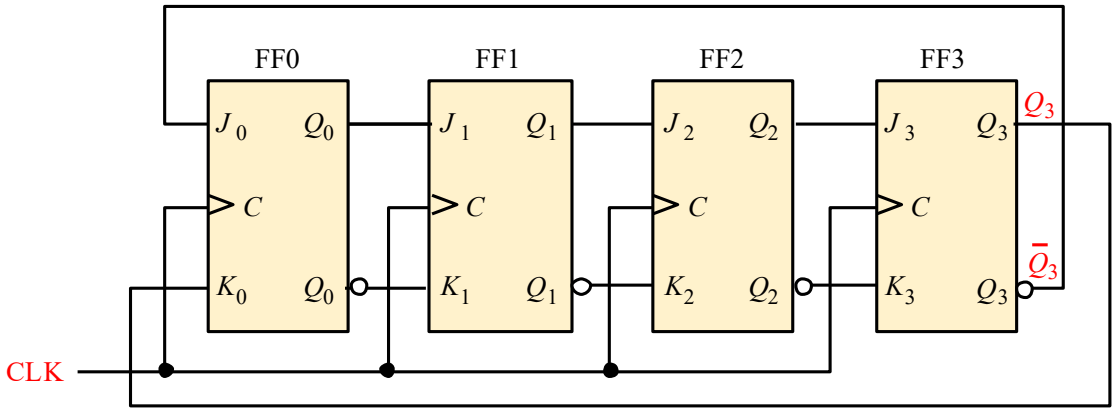
CLK	Q_0	Q_1	Q_2	Q_3
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1

The Johnson counter can be made with a series of D flip-flops

Shift Registers

Inputs			Outputs		
J	K	CLK	Q	$\overline{Q}$	Comments
0	0	↑	Q_0	$\overline{Q}_0$	No change
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	$\overline{Q}_0$	Q_0	Toggle

Johnson Counter



CLK	Q_0	Q_1	Q_2	Q_3
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1

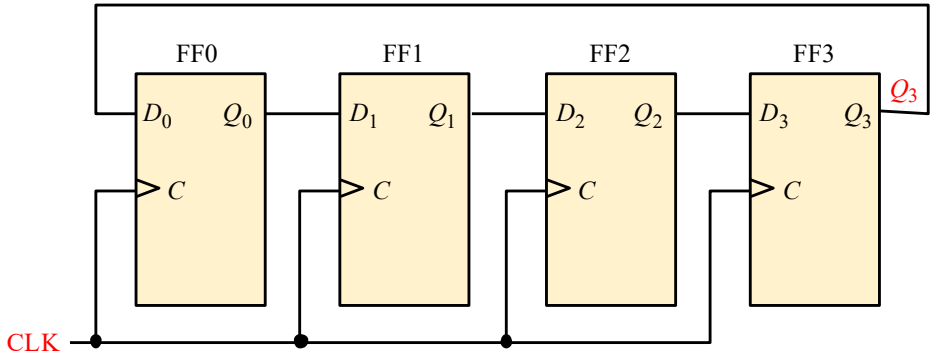
… or with a series of J-K flip flops. Here Q_3 and $\overline{Q_3}$ are fed back to the J and K inputs with a "twist".

Shift Registers

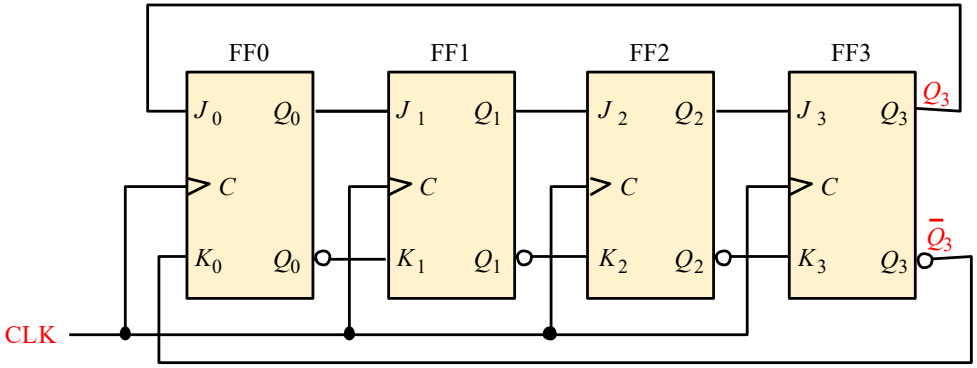
Ring Counter

The ring counter can also be implemented with either D flip-flops or J-K flip-flops.

Here is a 4-bit ring counter constructed from a series of D flip-flops.
Notice the feedback.



Like the Johnson counter, it can also be implemented with J-K flip flops.



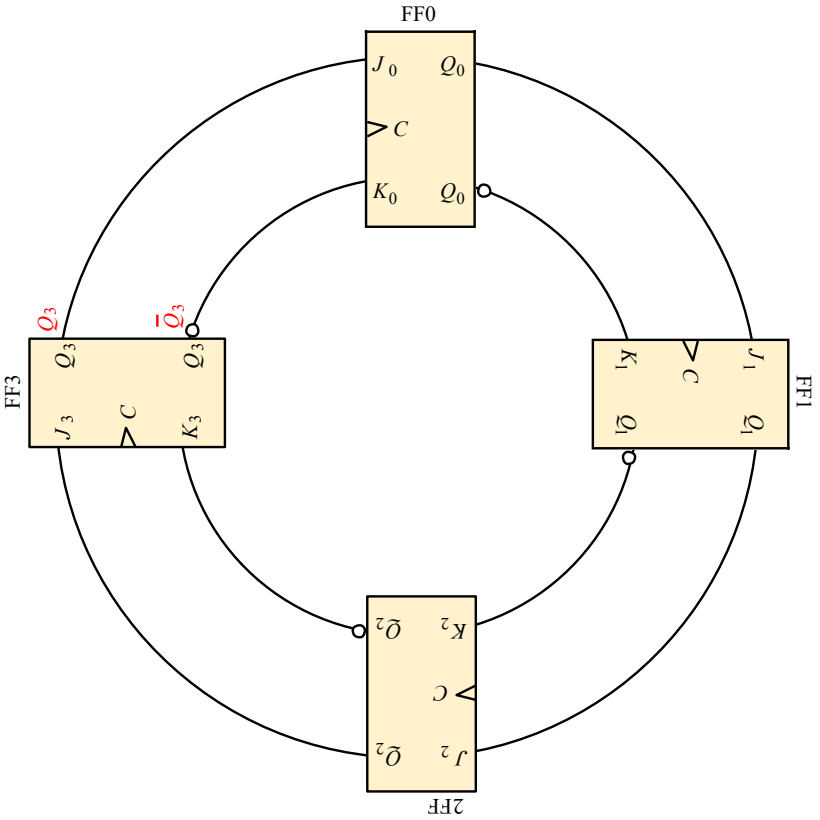
Shift Registers

Ring Counter

Redrawing the Ring counter (without the clock shown) shows why it is a "ring".

The disadvantage to this counter is that it must be preloaded with the desired pattern (usually a single 0 or 1) and it has states number (n, where n = number of flip-flops.

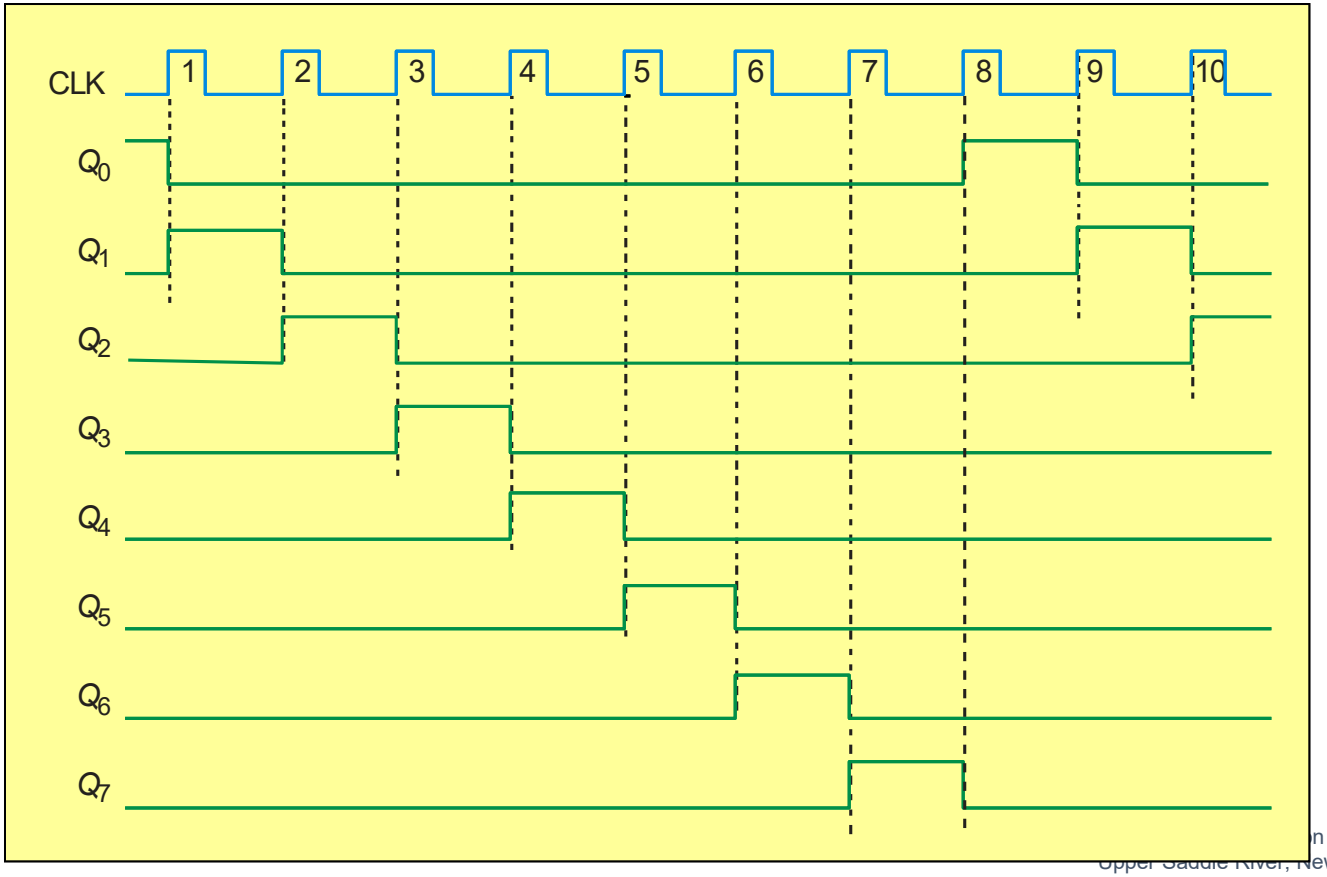
On the other hand, it has the advantage of being self-decoding with a unique output for each state.



Shift Registers

Ring Counter

A common pattern for a ring counter is to load it with a single 1 or a single 0. The waveforms shown here are for an 8-bit ring counter with a single 1.



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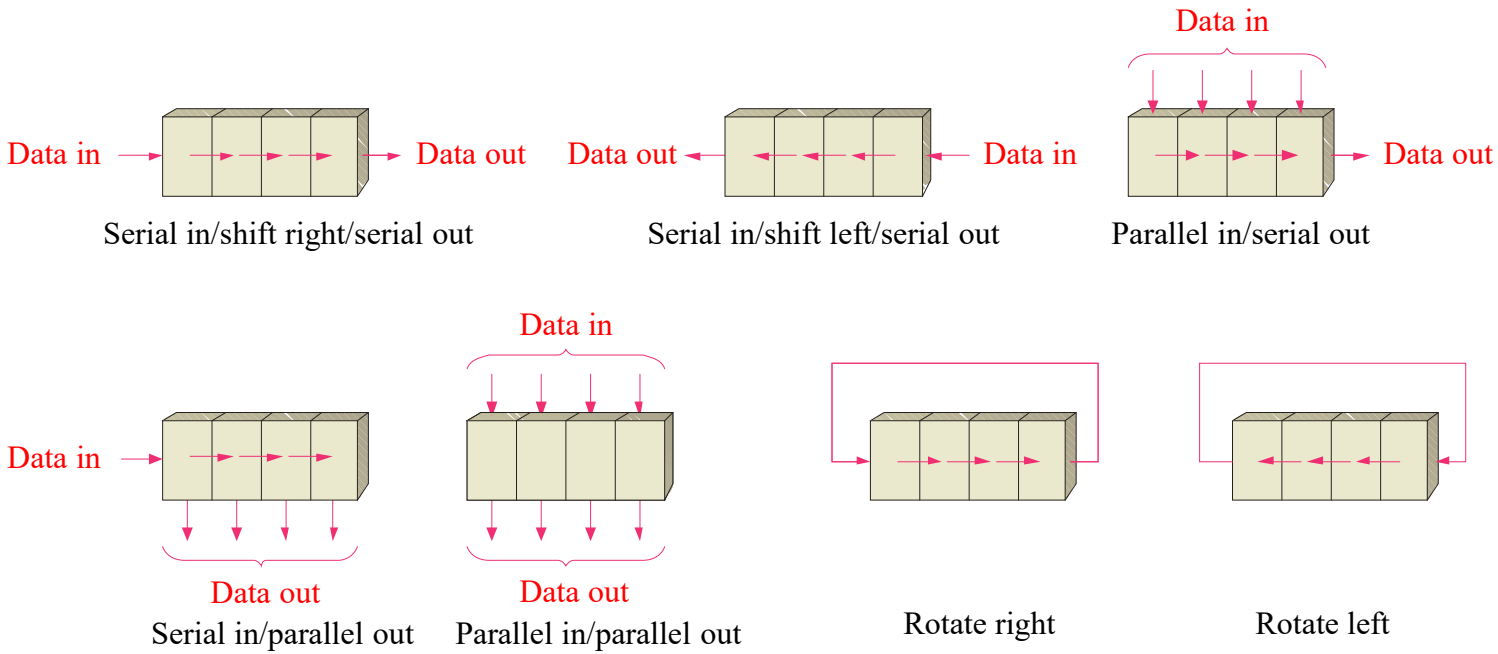
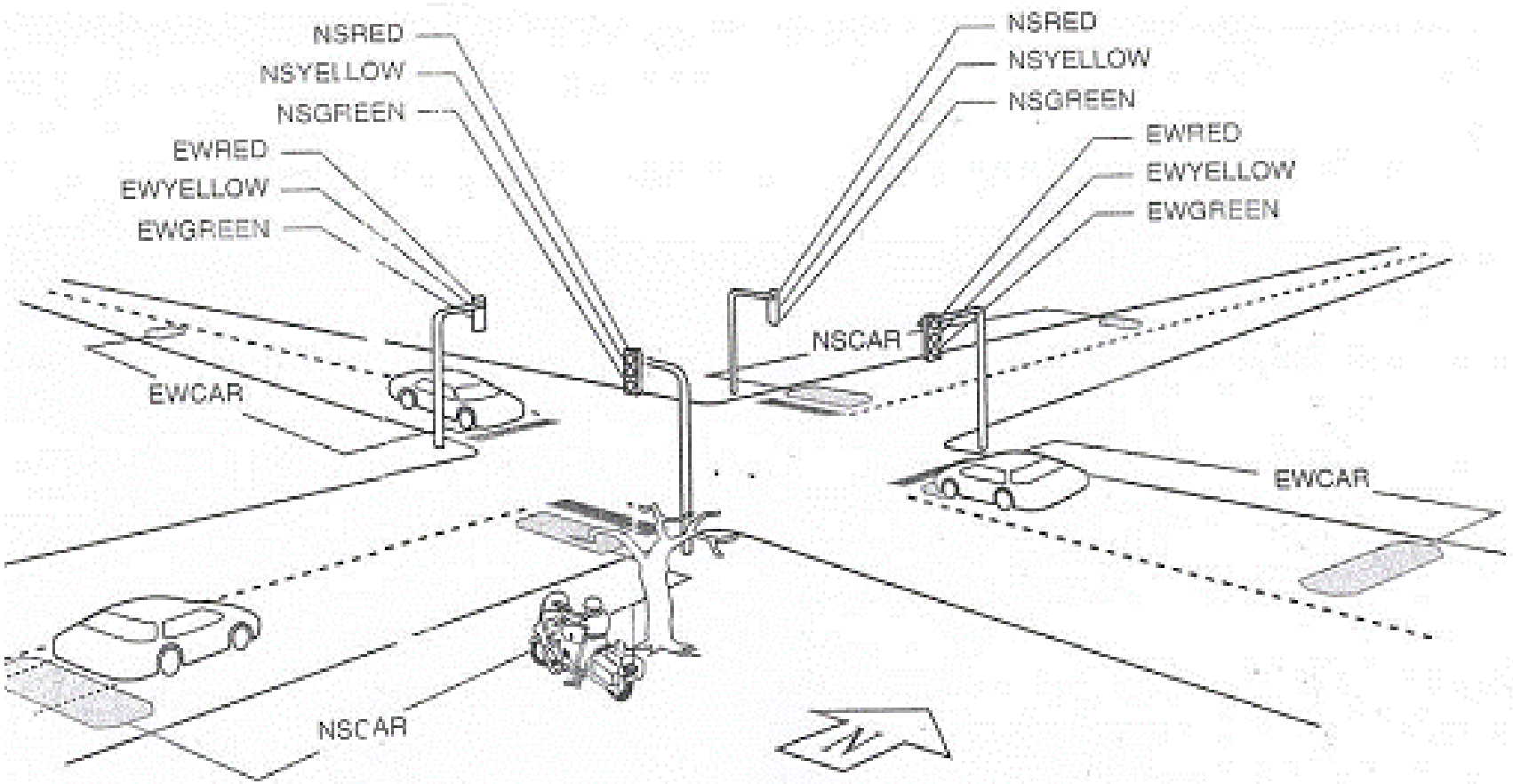


Application: Traffic Light Controller



Application: Traffic Light Controller